# Ultrafast all-optical logic gate using a nonlinear optical loop mirror based multi-periodic transfer function

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**Abstract:** A complete set of all-optical logic gate operations using a nonlinear-optical-loop-mirror-based multi-periodic transfer function is proposed. This scheme can operate all of sixteen two-input logic operations without changing configuration. We experimentally demonstrate AND, NAND, OR, NOR, XOR, and XNOR operations at 40 Gbit/s in a single configuration. We investigate the limitation of processing speed, and numerical simulation will show the feasibility of the processing speed up to 350 Gbit/s.



**OCIS codes:** (070.4340) Nonlinear optical signal processing; (200.4660) Optical logic

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## 1. Introduction

Recently, the demand for ultrafast signal processing is dramatically increasing. To increase the bit rate of an optical transmission system and realize an optical time division demultiplexer, ultrafast optical AND gate devices have been studied [1]. Also, in future photonic burst and packet switch networks, the photonic routers are expected to handle XOR operations for optical label swapping and header reconfiguration [2-4]. Generally speaking, the realization of various logic operations for ultrafast signals is essential for coming future applications.

Several approaches have been proposed to realize all-optical logic gates using semiconductor optical amplifiers (SOA) and highly nonlinear optical fibers (HNLF) [5-8]. The schemes using HNLF have advantages in that ultrafast optical signals can be processed through the femtosecond response of Kerr effect in silica [9]. However, HNLF tend to be large in size if integration is attempted, in contrast to those using integrated SOAs. Therefore, in order to be useful with such a difficulty of the HNLF-based schemes, one must seek a scheme such that one fixed configuration can provide as many logic operations as possible.

In order to provide flexibility, and to simplify the configuration, the variable logic gates capable of many logic operations have been proposed [6-8]. We have also proposed and demonstrated an all-optical logic gate that is capable of six basic logic operations (AND, NAND, OR, NOR, XOR, and XNOR) using a nonlinear optical loop mirror (NOLM) [10]. In [10], multi-periodic transfer functions of the NOLM were essential. Indeed, we have investigated and realized such NOLM operations through the studies on NOLM-based ultrafast all-optical analog-to-digital conversion (ADC) [11-13]. In this paper, we claim that none of the previously reported schemes has realized all two-input logic operations in the same configuration. Here, we propose and experimentally demonstrate a versatile all-optical logic gate capable of all sixteen two-input logic operations without changing the configuration. We then consider the limitation of the processing speed due to dispersion and undesirable nonlinear effects in HNLF. The experimental demonstrations are all-optical logic operations of AND, NAND, OR, NOR, XOR, and XNOR at 40 Gbit/s. We show the feasibility of the processing speed up to 350 Gbit/s by numerical simulation.

## 2. Operating principle of all-optical logic gate

The configuration of the proposed optical logic gate is shown in Fig. 1. The logic gate operation is realized through a bidirectional-input NOLM-based switch and a thresholder/limiter. The thresholder/limiter follows this switch in order to eliminate the incomplete suppression of nulls and non-uniform height of ones for the sake of the sinusoidal nature of NOLM switching. The input RZ signals X and Y at a wavelength of $\lambda_1$ are launched into the loop via the WDM couplers as clockwise and counter-clockwise travelling control pulses, respectively. The output is obtained from either Port T or Port R depending on the type of logic operation to be realized. The variable attenuators (VOAs) are used to adjust the input powers. The transfer function of the NOLM switch depends on the differential phase shift

$$\Delta\phi = |\phi_{CW} - \phi_{CCW}|. \quad (1)$$

where $\phi_{CW}$ and $\phi_{CCW}$ are defined as the phase shift induced by the input signals X and Y,

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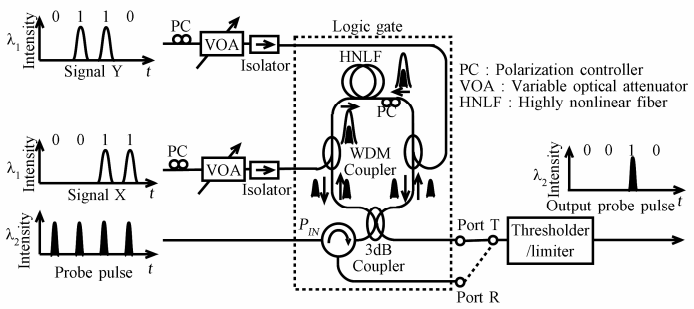


Fig. 1 Configuration of versatile all-optical logic gate.

Table 1 Phase shift amount for all two-input logic operation.

| Logic operation | $\phi_{CW}$ [rad] | $\phi_{CCW}$ [rad] | Output port | Output level (Output power) at input signal X:Y | | | |
|---|---|---|---|---|---|---|---|
| | | | | 1:1 | 1:0 | 0:1 | 0:0 |
| 0 | 0 | 0 | Port T | 0 (0) | 0 (0) | 0 (0) | 0 (0) |
| $\overline{X+Y}$ (NOR) | 2π/3 | 4π/3 | Port R | 0 (0.25$P_{IN}$) | 0 (0.25$P_{IN}$) | 0 (0.25$P_{IN}$) | 1($P_{IN}$) |
| $\overline{X}\bullet Y$ | π/3 | 2π/3 | Port T | 0 (0.25$P_{IN}$) | 0 (0.25$P_{IN}$) | 1 (0.75$P_{IN}$) | 0 (0) |
| $\overline{X}$ | π | 0 | Port R | 0 (0) | 0 (0) | 1 ($P_{IN}$) | 1 ($P_{IN}$) |
| $X\bullet\overline{Y}$ | 2π/3 | π/3 | Port T | 0 (0.25$P_{IN}$) | 1 (0.75$P_{IN}$) | 0 (0.25$P_{IN}$) | 0 (0) |
| $\overline{Y}$ | 0 | π | Port R | 0 (0) | 1 ($P_{IN}$) | 0 (0) | 1 ($P_{IN}$) |
| $X\oplus Y$ (XOR) | π | π | Port T | 0 (0) | 1 ($P_{IN}$) | 1 ($P_{IN}$) | 0 (0) |
| $\overline{X\bullet Y}$ (NAND) | π/3 | 5π/3 | Port R | 0 (0.25$P_{IN}$) | 1 (0.75$P_{IN}$) | 1 (0.75$P_{IN}$) | 1 ($P_{IN}$) |
| $X\bullet Y$ (AND) | π/3 | 5π/3 | Port T | 1 (0.75$P_{IN}$) | 0 (0.25$P_{IN}$) | 0 (0.25$P_{IN}$) | 0 (0) |
| $\overline{X\oplus Y}$ (XNOR) | π | π | Port R | 1 ($P_{IN}$) | 0 (0) | 0 (0) | 1 ($P_{IN}$) |
| $Y$ | 0 | π | Port T | 1 ($P_{IN}$) | 0 (0) | 1 ($P_{IN}$) | 0 (0) |
| $X+\overline{Y}$ | 2π/3 | π/3 | Port R | 1 (0.75$P_{IN}$) | 0 (0.25$P_{IN}$) | 1 (0.75$P_{IN}$) | 1 ($P_{IN}$) |
| $X$ | π | 0 | Port T | 1 ($P_{IN}$) | 1 ($P_{IN}$) | 0 (0) | 0 (0) |
| $\overline{X}+Y$ | π/3 | 2π/3 | Port R | 1 (0.75$P_{IN}$) | 1 (0.75$P_{IN}$) | 0 (0.25$P_{IN}$) | 1 ($P_{IN}$) |
| $X+Y$ (OR) | 2π/3 | 4π/3 | Port T | 1 (0.75$P_{IN}$) | 1 (0.75$P_{IN}$) | 1 (0.75$P_{IN}$) | 0 (0) |
| 1 | 0 | 0 | Port R | 1 ($P_{IN}$) | 1 ($P_{IN}$) | 1 ($P_{IN}$) | 1 ($P_{IN}$) |

respectively. For example, when signal X is “1” level, the clockwise travelling probe pulse induces a phase shift due to the cross phase modulation (XPM) in HNLF. For signal Y at “1” level, the counter-clockwise travelling probe pulse also induces a phase shift. The phase shifts become null for the cases of “0” signal inputs. The peak powers of the output probe pulses can be written as

$$P_{OUTT} = P_{IN}(1-\cos\Delta\phi)/2, \quad (2)$$

$$P_{OUTR} = P_{IN}(1+\cos\Delta\phi)/2, \quad (3)$$

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where $P_{IN}$ is the peak power of the input probe pulse, $P_{OUTT}$ and $P_{OUTR}$ are the peak powers of the output probe pulses at the transmission and reflection ports, respectively. A variety of

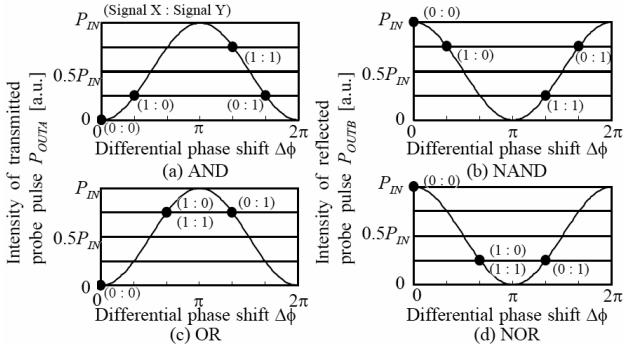


Fig. 2. Variable logic operation.

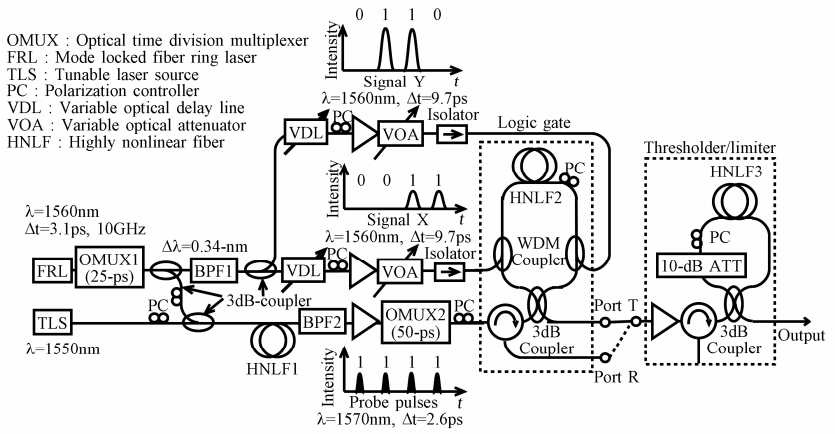


Fig. 3. Experimental setup.

logic operations can be realized by properly setting the values of the phase shifts $\phi_{CW}$ and $\phi_{CCW}$, that are in proportion with the peak power of the input signals. The phase shifts due to the input "1" signal for all two-input logic functions are summarized in Table 1. For example, Fig. 2 shows the transfer functions and operating points of NOLM for logic operations of AND, NAND, OR, and NOR. The output of OR operation is obtained from the transmission port $P_{OUTT}$ by setting the phase shifts $\phi_{CW}$ and $\phi_{CCW}$ to be $2\pi/3$ rad and $4\pi/3$ rad, respectively. Note that the input peak powers are represented in two ways, the logical values 0 or 1 and the actual values in the bracket. When, input signals (X:Y) are (0:0), (0:1), (1:0), and (1:1), the peak powers of transmitted probe pulse $P_{OUTT}$ becomes 0, $0.75P_{IN}$, $0.75P_{IN}$, and $0.75P_{IN}$, respectively as shown in Fig. 2(c).

## 3. Experimental setup and results

Figure 3 shows the experimental setup for the all-optical logic gate operating at 40 Gb/s. We used a 10-GHz mode-locked fiber ring laser (FRL) operating at a wavelength of 1560 nm and a time width of 3.1 ps. The first optical time division multiplexer (OMUX1) with a time interval of 25 ps generates control pulse sequences of {0011} and {0110} at 40 Gb/s. We generate probe pulses from wavelength conversion of the control pulses in $HNLF_1$ through the degenerate four-wave mixing with the continuous wave signal light of 1550 nm tunable laser source (TLS). And the following OMUX2 with 50-ps time interval generates a pulse sequence of {1111} at 40 Gb/s. The probe pulses have a carrier wavelength of 1570 nm, a pulse width of 2.6 ps, and are synchronized with the signal pulse bit sequences. The BPF1 with 3-dB

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bandwidth of 0.34 nm was used to expand the width of each control pulse up to 9.7 ps. The variable optical delay lines (VDL) were adjusted for fixed signal pattern of (X:Y) = (0:0),

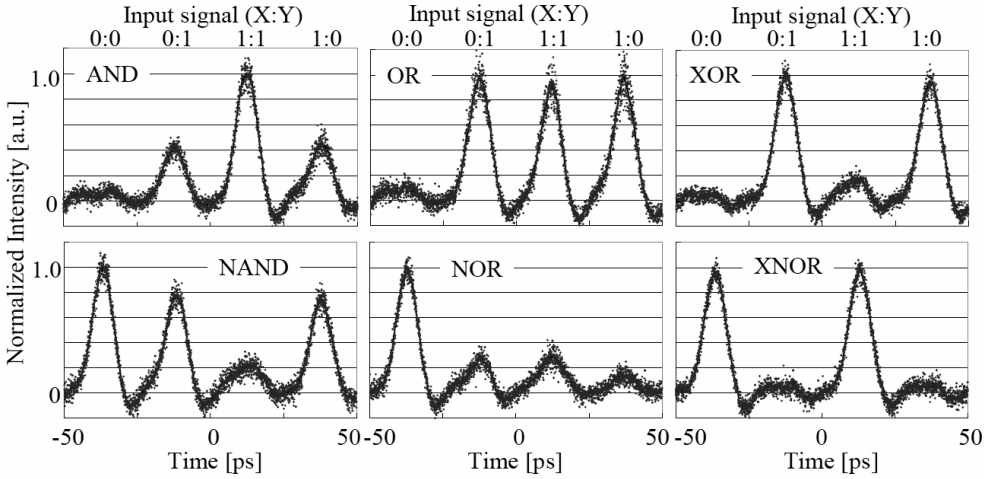


Fig. 4. Sampling oscilloscope traces of output probe pulse in each logic operation before the thresholder/limiter.

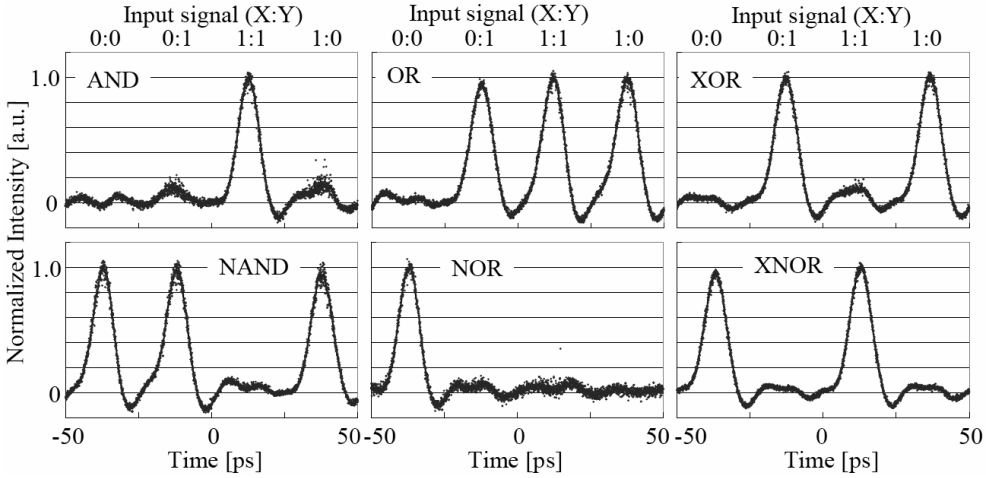


Fig. 5. Sampling oscilloscope traces of output probe pulse in each logic operation after the thresholder/limiter.

Table 2 Extinction ratios in each logic operation before and after the thresholder/limitter.

| Logic operation | Before | After | Logic operation | Before | After |
|---|---|---|---|---|---|
| AND | 3.5 dB | 8.6 dB | NAND | 5.4 dB | 13.1 dB |
| OR | 9.2 dB | 14.9 dB | NOR | 5.4 dB | 11.7 dB |
| XOR | 7.5 dB | 9.4 dB | XNOR | 12.3 dB | 13.8 dB |

(0:1), (1:1), and (1:0) at each time slot. The peak powers of input signals X and Y are adjusted to the phase shifts $\phi_{CW}$ and $\phi_{CCW}$ of each logic operation by the VOAs, as shown in table 2. The fiber length L and the nonlinear coefficient $\gamma$ of $HNLF_2$ of the logic gate were 380 m and 17.5 $W^{-1}km^{-1}$, respectively. The second-stage NOLM was used as a thresholder/limiter. The

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Table 3 Simulation parameters.

| HNLFs parameters | | |
|---|---|---|
| | $HNLF_1$ | $HNLF_2$ |
| Fiber loss [dB/km] | 0.5 | 0.5 |
| Zero dispersion wavelength $\lambda_0$ [nm] | 1565 | 1576.5 |
| Dispersion slope [ps/km-nm$^2$] | 0.02 | 0.02 |
| Nonlinearity [1/W-km] | 12.0 | 12.0 |
| Fiber length [km] | 0.5 | 0.5 |
| BPF parameters | | |
| Bandwidth [nm] | 5 | |
| Filter shape | Gaussian | |
| Probe pulse parameters | | |
| Pulse width [ps] | 0.5 | |
| Pulse shape | Sech | |
| Peak power [W] | 0.01 | |

Table 4 wavelength spacing and peak powers.

| Initial pulse width [ps] | Wavelength spacing $\Delta\lambda$ [nm] | Peak power [W] | |
|---|---|---|---|
| | | Signal X | Signal Y |
| 0.5 | 36 | 0.20 | 1.18 |
| 0.6 | 30 | 0.16 | 0.96 |
| 0.7 | 26 | 0.14 | 0.82 |
| 0.8 | 23 | 0.13 | 0.75 |
| 0.9 | 21 | 0.12 | 0.69 |
| 1.0 | 20 | 0.12 | 0.68 |
| 1.1 | 18 | 0.11 | 0.65 |

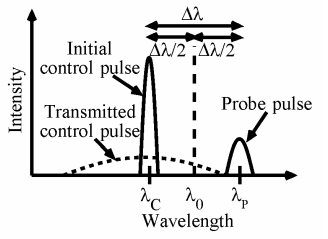


Fig. 6. Wavelength allocation.

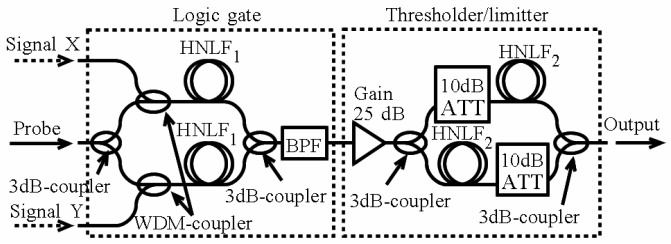


Fig. 7. Simulation model.

gain of EDFA and PC in the thresholder/limiter were adjusted to suppress "0" level signals, and stabilizing fluctuations of "1" level signals. The fiber length L and the nonlinear coefficient $\gamma$ of $HNLF_3$ were 830 m and 19 $W^{-1}km^{-1}$, respectively.

Figures 4 and 5 show the waveforms of output probe pulses before and after the thresholder/limiter, respectively. Table 2 shows the extinction ratios of output probe pulses before and after the thresholder/limiter, respectively. These waveforms were measured with a photo detector and a sampling oscilloscope. The logic operations AND, NAND, OR, NOR, XOR, and XNOR were successfully obtained, as the thresholder/limiter suppressed "0" level signals and tailored "1" level signals. The extinction ratios were improved to over 8.6 dB by the tresholder/limiter. We note that the width of the output probe pulse from the logic gate and the thresholder/limiter measured with an autocorrelater was 2.8 ps. The pulse widths in figures 4 and 5 were wider than 2.8 ps, due to the limited bandwidth of the photo detector and the sampling oscilloscope.

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## 4. Discussion

In this section, we discuss the limitation of processing speed due to group velocity dispersion (GVD) and self-phase-modulation (SPM) in HNLF. In order to suppress an inter-symbol interference (ISI), the time slot has to be wider than the pulse width of the control pulse

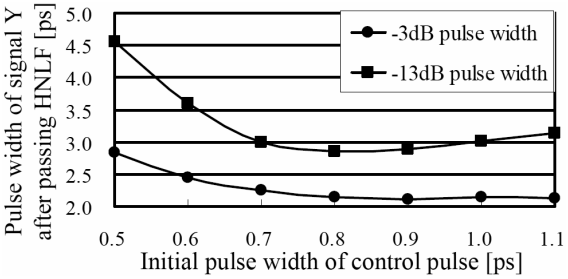


Fig. 8. Pulse width of signal Y after passing through the HNLF.

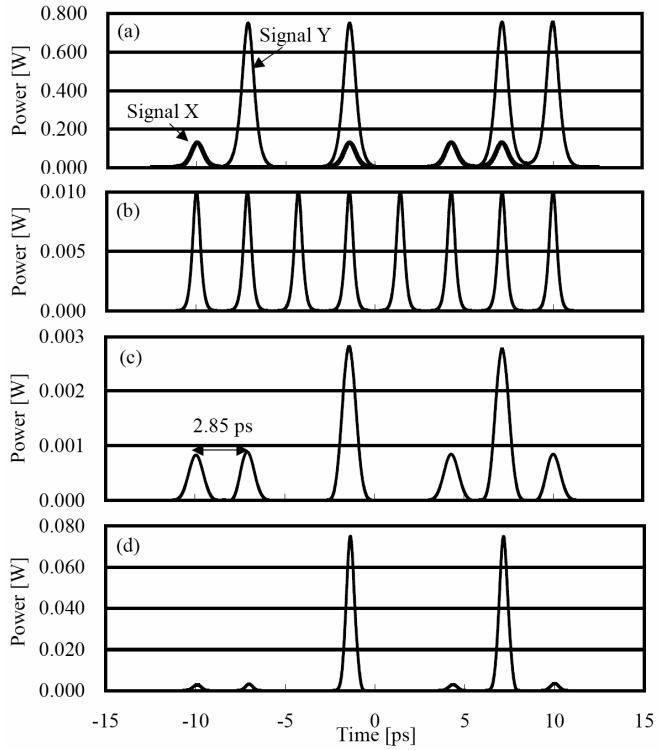


Fig. 9. Simulation result: Waveforms of (a) signal X and Y, (b) probe pulse, and (c) output signal before the thresholder/limiter, (d) output signal after the thresholder/limiter.

through the HNLF. The GVD has to be carefully designed for ultrafast operation, because the wavelengths of the control and probe pulses are allocated in normal and anomalous dispersion region in order to suppress walk-off effect, as shown in Fig. 6. The temporal shapes of the control pulses are also changed by the interaction of GVD and SPM. Therefore, we need to optimize the peak power and the pulse width of control pulses with respect to the dispersion profile and the nonlinearity of HNLF, while at the same time the spectral broadening of the control pulse caused by SPM has to be taken into account. If the wavelength spacing $\Delta\lambda$ between the control and probe pulse is too narrow, the broadened spectrum of the control

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pulse overlaps with that of the probe pulse. If the wavelength spacing is too wide, the control pulse is greatly broadened due to the large GVD.

We investigate the minimum time slot determined by the interaction of GVD and SPM for the parameters of a currently available HNLF by numerical simulation. Table 3 shows the parameters of HNLFs, a BPF and the probe pulse. Here, we simulated the case of AND operation, because AND and NAND operations are the most difficult ones due to the largest phase shift of $5\pi/3$. Figure 7 shows the simulation model of the logic gate and the thresholder/limitter. In order to consider the GVD and nonlinearity in a HNLF, we used split-step-Fourier-method. To simplify the simulation procedure, we split the counter-clockwise and clockwise path into two different paths. Table 4 shows the minimum wavelength spacing to avoid overlap of the broadened spectrum of the control pulse, and the peak powers of signals X and Y at each initial pulse width. Figure 8 shows the -3 dB and -13 dB pulse width of signal Y after passing through the HNLF against the initial pulse width. The shape of a control pulse becomes nearly rectangular due to an interaction of the GVD and nonlinear effect. Therefore, the width of time slot can set shorter than twice -3dB width without the effect of ISI. Here, we define the -13 dB pulse width of transmitted signal Y as the minimum width of a time slot, because the powers of output probe pulses with the effect of the bit pattern are stable enough. The -13 dB width has the minimum value of 2.85 ps when the initial pulse width is 0.8 ps. The processing speed can be up to 350 Gbit/s with currently available HNLF. Figure 9 shows the input and output waveforms of the AND operation for the input pulse with a temporal width of 0.8 ps, and for a processing speed of 350 Gbit/s. Theses results show that the ISI effect in the logic gate is very small. The extinction ratio of output probe pulses was improved to 13.7 dB from 5.0 dB by the thresholder/limitter. The processing speed can be future improved by decreasing the dispersion slope of the HNLF.

## 5. Conclusions

We have proposed a versatile all-optical logic gate based on multi-periodic transfer function of a NOLM. We have shown that the proposed scheme can perform all sixteen two-input logic operations only by adjusting PCs and VOAs without changing the configuration. We have also experimentally demonstrated all-optical AND, NAND, OR, NOR, XOR, and XNOR operations at the processing speed of 40 Gbit/s. It has been found that the control and probe pulses with short temporal widths and a carefully designed wavelength allocation are required for realizing a ultrafast logic gate. We show the feasibility of the processing speed up to 350 Gbit/s by numerical simulation.

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